AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph on page 9 beginning on line 9 as follows:

The differential address input unit includes a first input NMOS transistor M23 whose gate receives the reference voltage VREF and a second input NMOS transistor ~~M23~~ M22 whose gate receives the input address signal AIN. Also, the current mirroring unit includes load PMOS transistors M24 and M25, which are connected between the power supply voltage VDD and the input NMOS transistors M22 and M23, forming a current mirror circuit. The biasing unit includes a bias NMOS transistor M21 whose gate receives an output signal bias_ctrl. The bias NMOS transistor M21 is commonly connected between the ground voltage VSS and the input transistors M22 and M23.

AMENDMENTS TO THE ABSTRACT

Please replace the Abstract Of The Disclosure with the following new Abstract Of The Disclosure. Applicant also submits the Abstract Of The Disclosure on a separate page.

An address input buffer in a semiconductor memory device. The address buffer has a differential amplifying device for differentially amplifying a reference voltage and an external address signal, and a controlling device for generating a bias control signal by receiving a refresh signal and a bank active signal to control the differential amplifying device. Activation of the bias control signal depends on the bank active signal when the refresh signal is abnormally activated in an initialization process.